Coating Parameter vs. Stress

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Structure zone model

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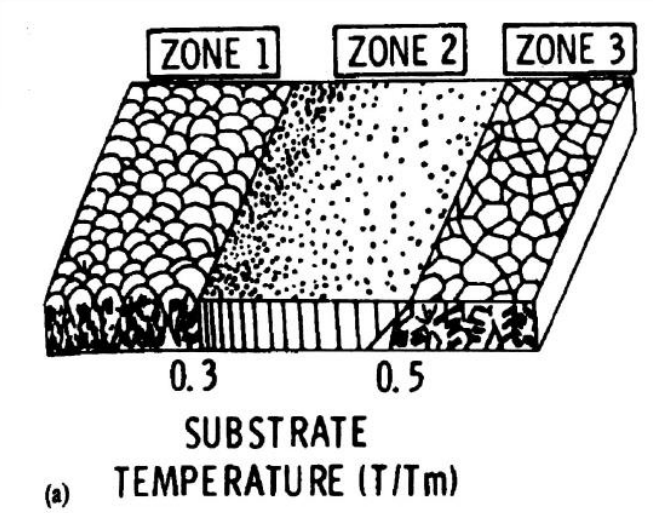
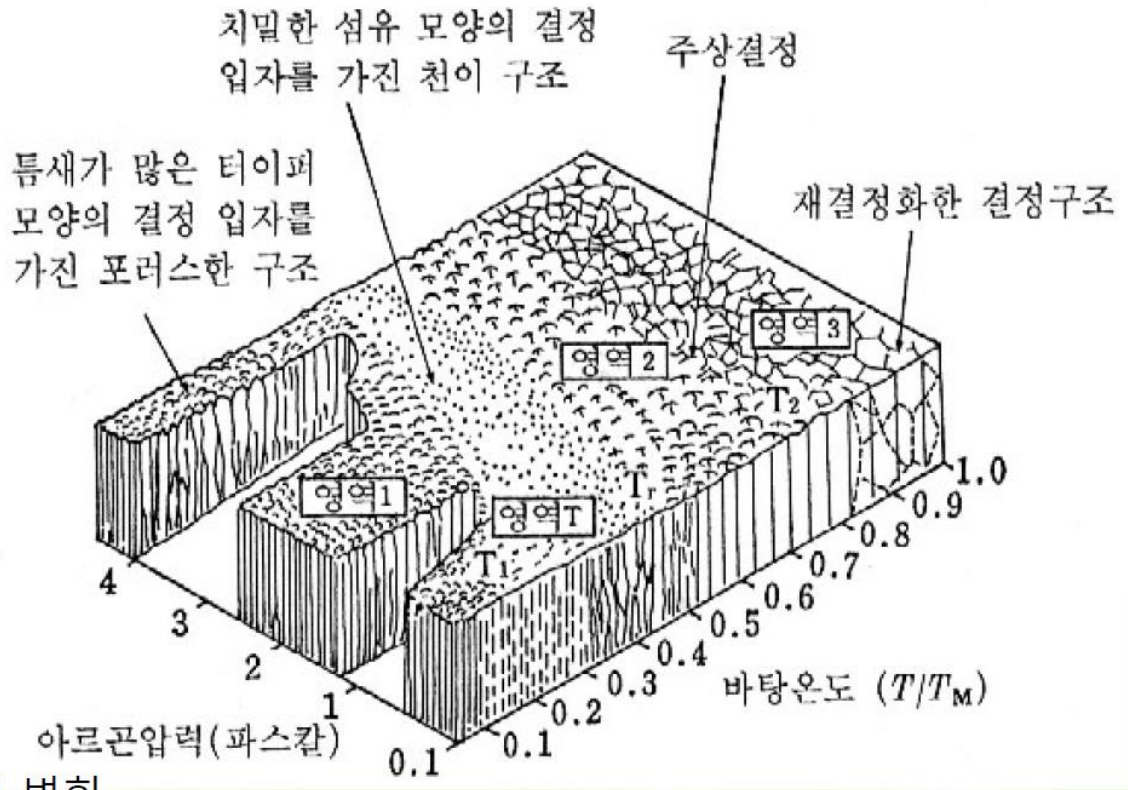
기판의 온도 및 압력이 낮을수록, 결정성 및 지밀성의 변화 ➔ 에너지 관점





압력의 변화
➔ 평균 자유행정거리의 변화
➔ 기판에 도달하는 입자의 에너지 변화

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Advanced Structure zone model

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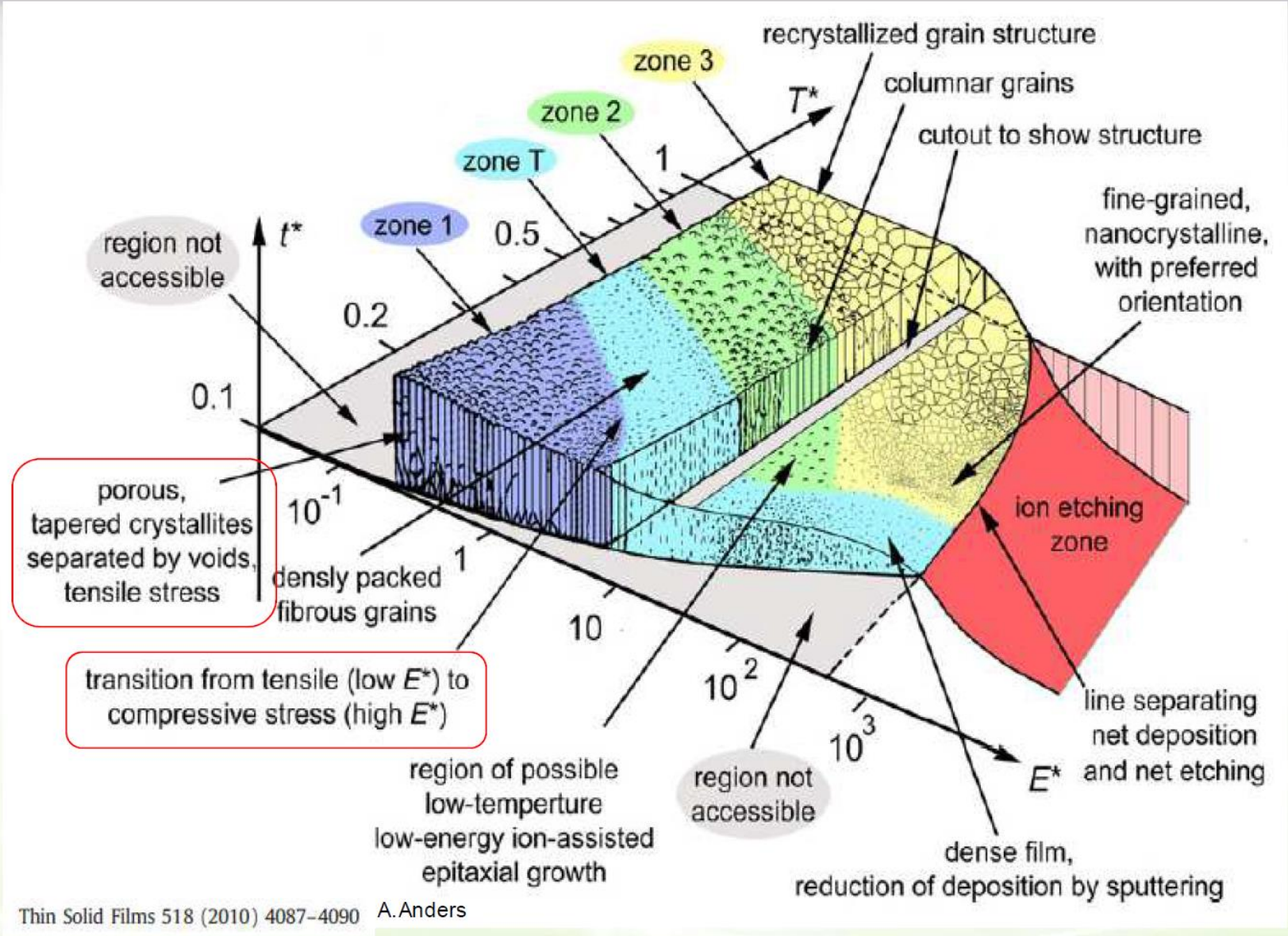

Thin Solid Films 518 (2010) 4087–4090 A.Anders

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Residual Stress of Thin Films

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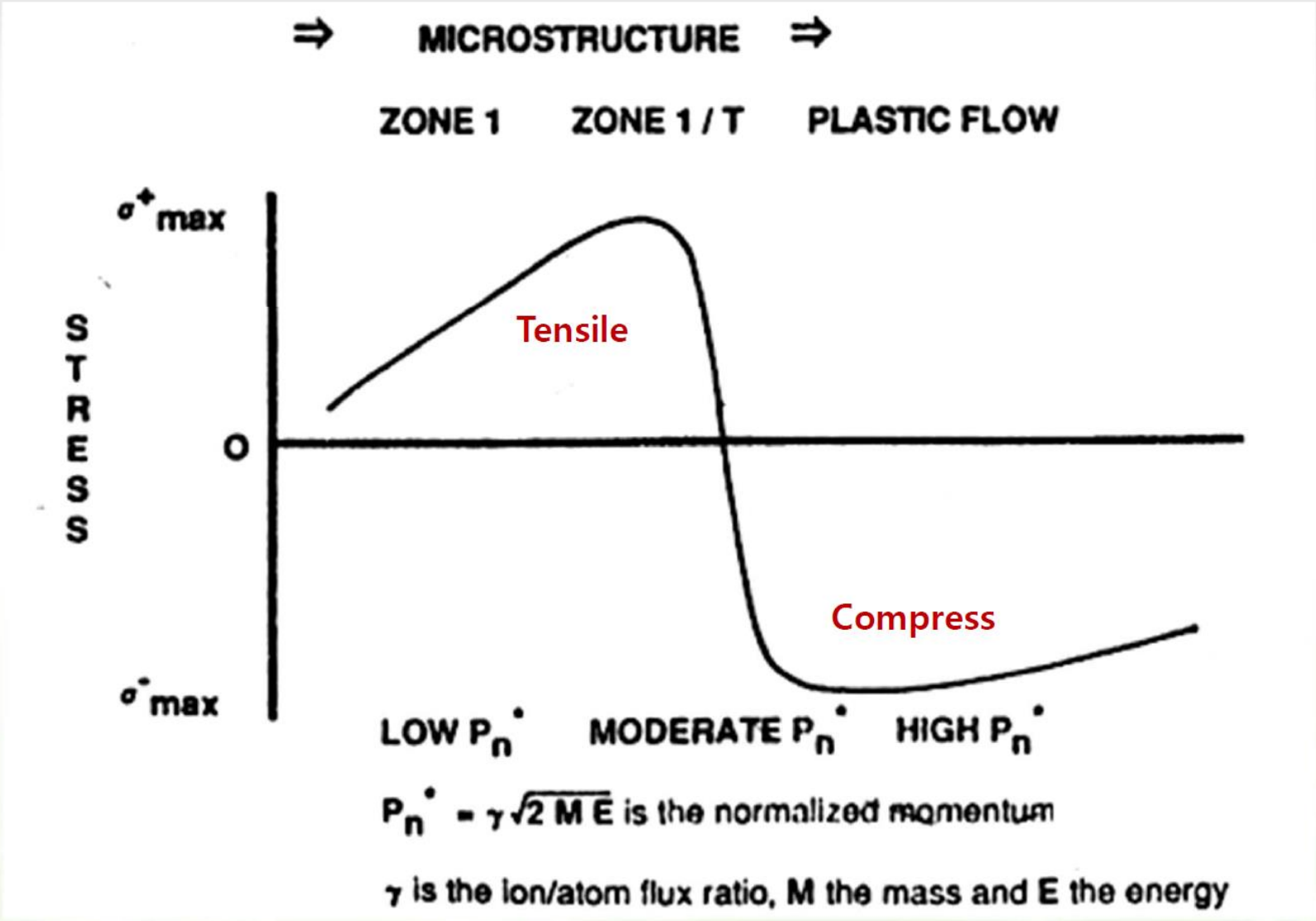

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Intrinsic Stress (Growth Stress)

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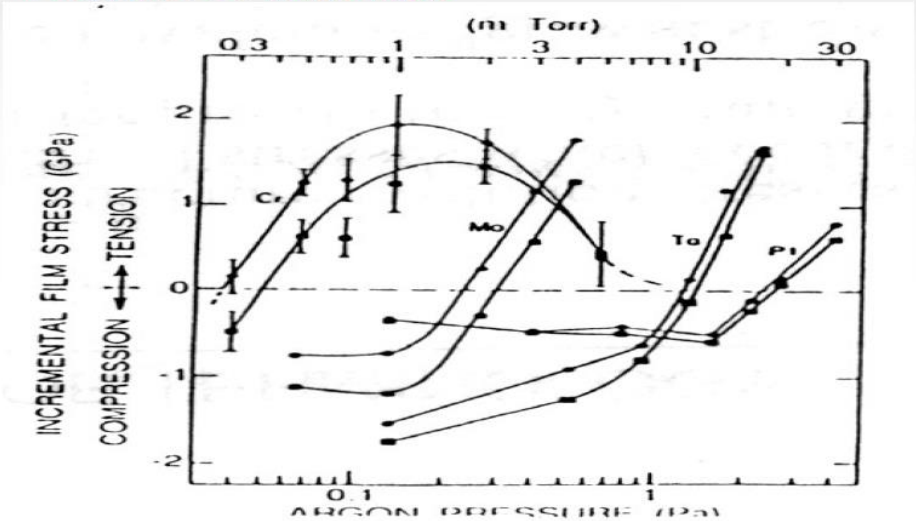
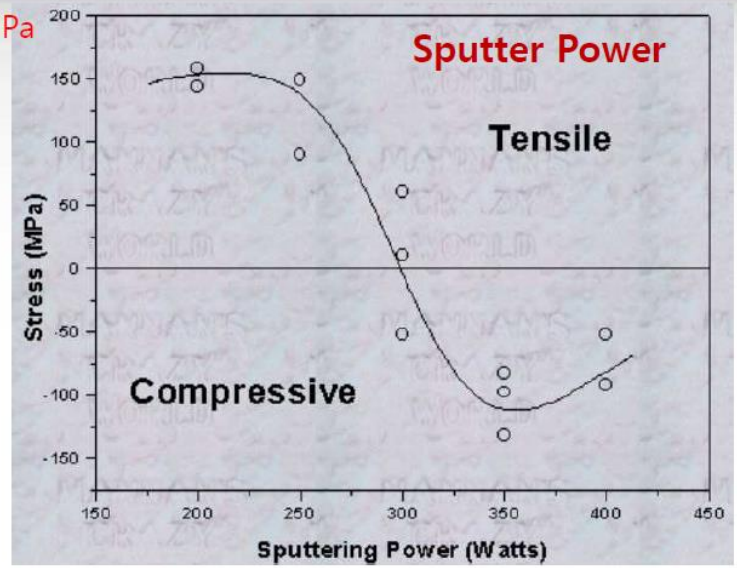
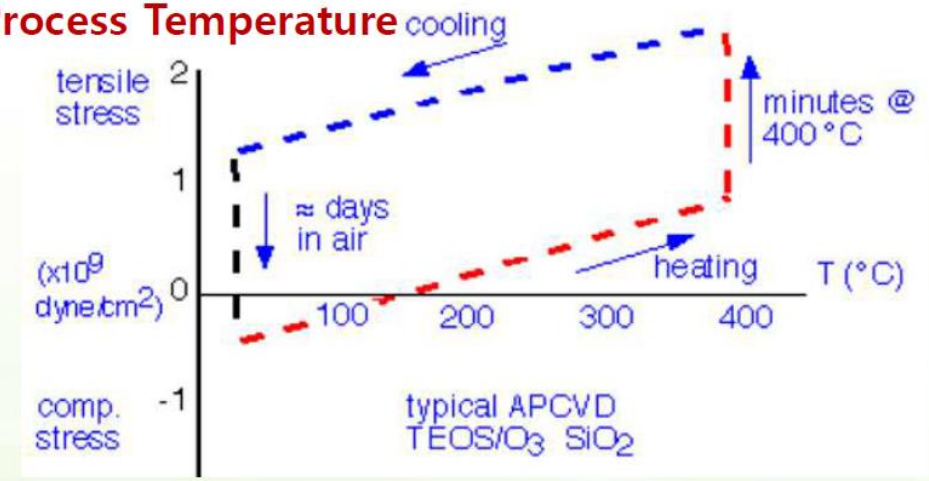
Pressure & Materials



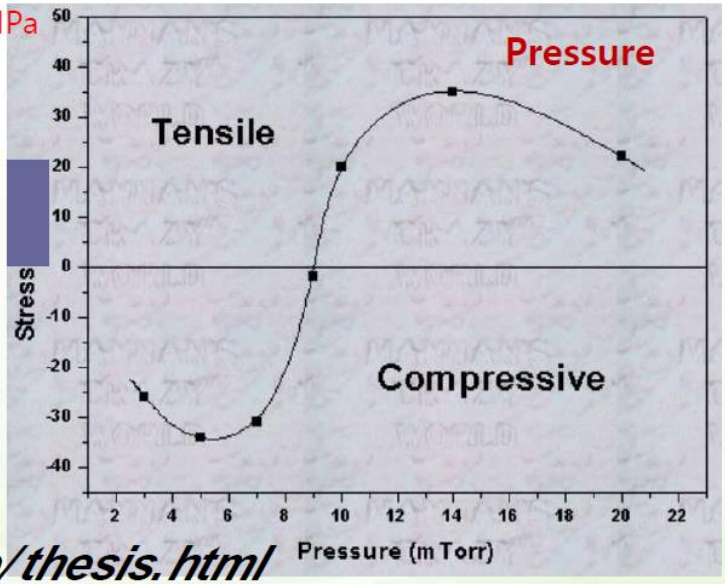
200 MPa



Process Temperature



50 MPa



Web: http://members.xoom.com/MannansZone/thesis.html

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Thick ta-C coating

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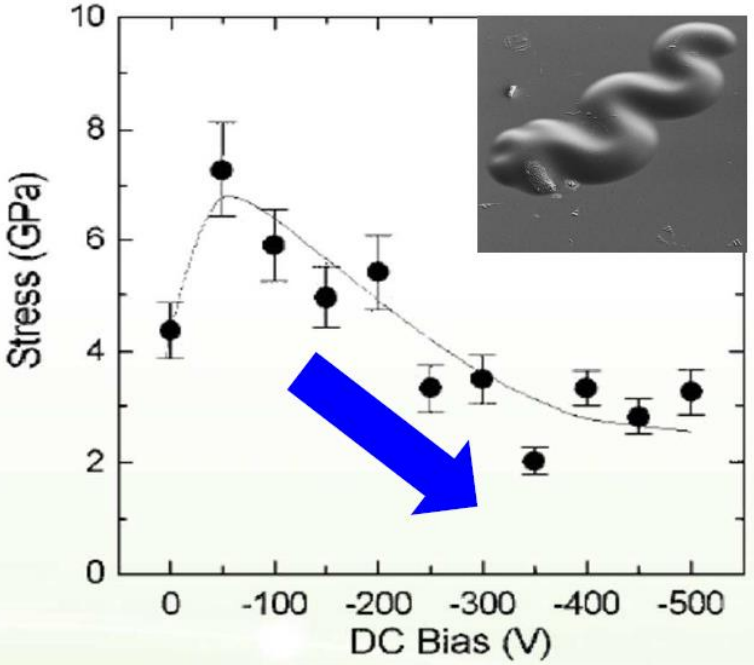
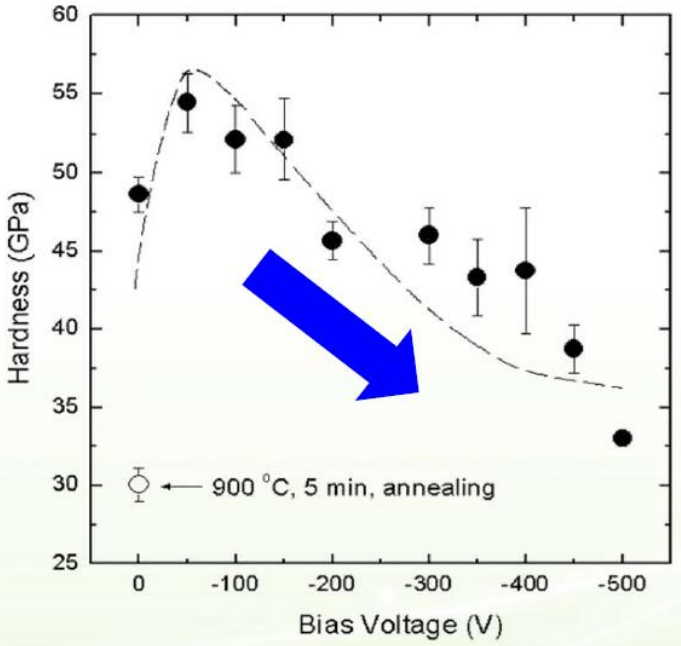
- **Aim : How to make THICK ta-C coating (>1um) with "low stress" & "high hardness" ?**
- **KIMS approach : Parameters control in FVAS process**
  - Arc current, Gas flow rate(Pressure), Substrate bias, Deposition temp.



Stress behaviors as a function of DC bias



Hardness behaviors as a function of DC bias

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Ta-C Thicken

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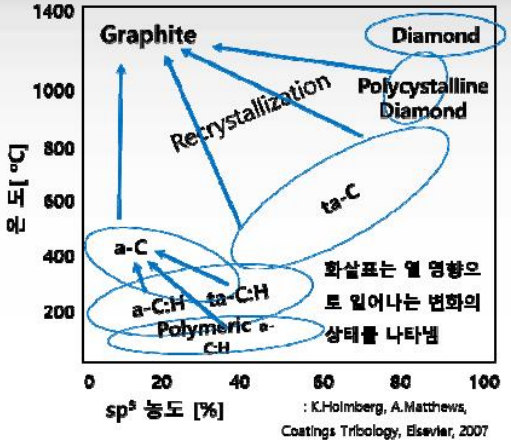
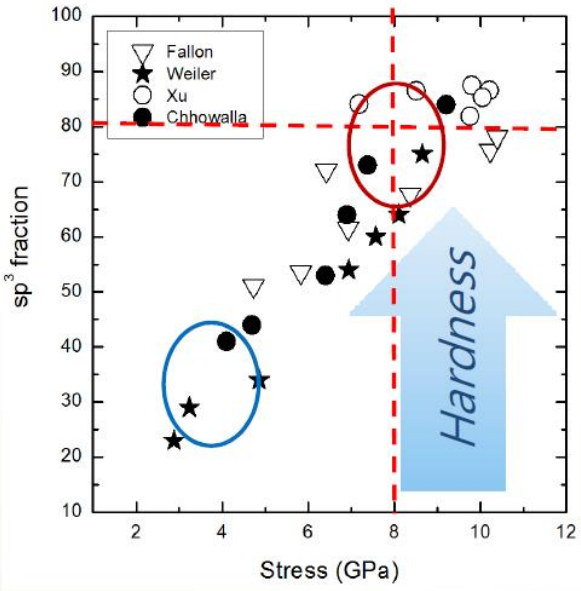
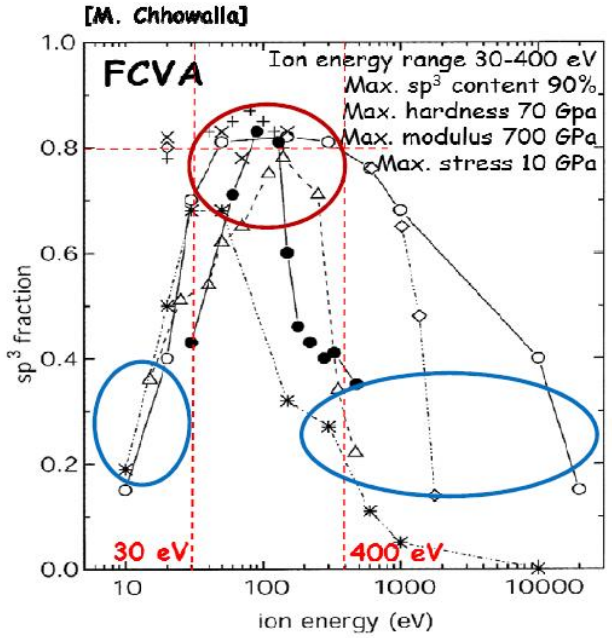
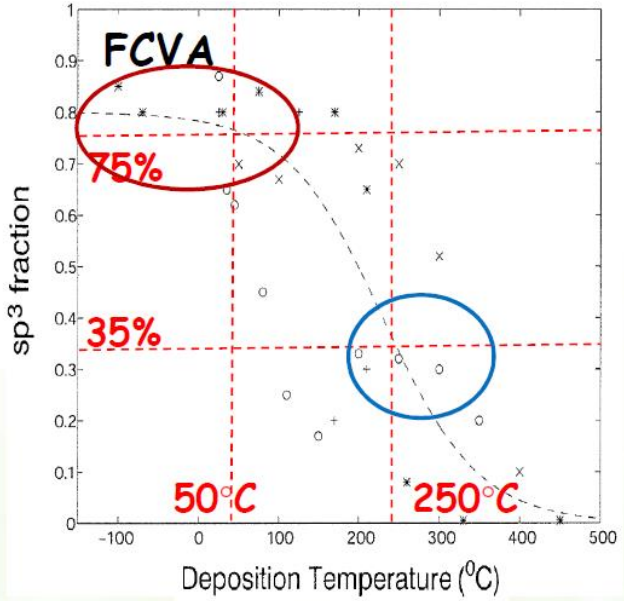
- **Process Parameter (Bias, Temperature, Pressure)**
  - High Energy ➔ Graphitization
  - Poor buffer ➔ Low adhesion









- High Hardness=High Stress , High Sp3 fraction, Low process Temperature, Bias(DC30-100 eV)
- Low Hardness=low Stress, Low SP3 fraction, High Process Temperature, High Bias Voltage

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Mechanical properties

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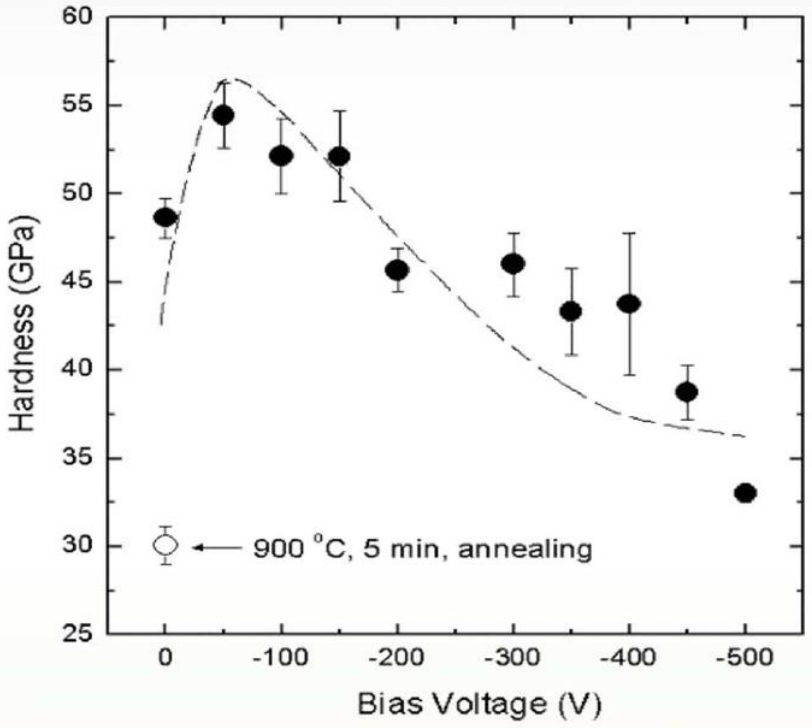
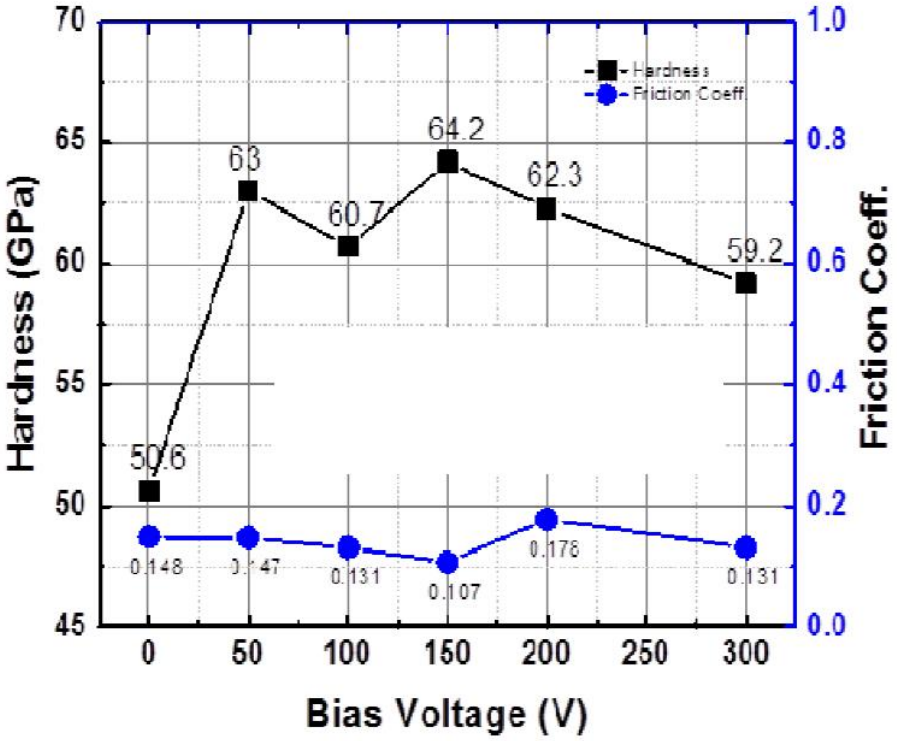
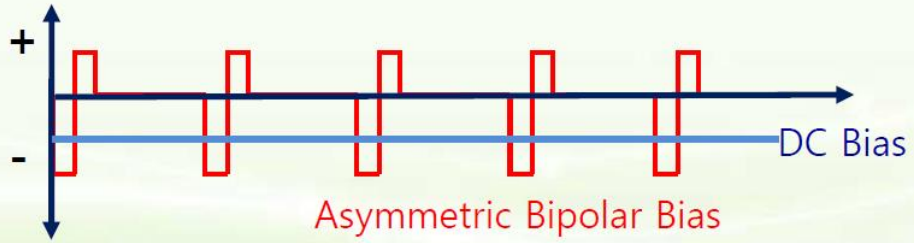
Only DC Bias



Asymmetric Bipolar Bias





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ta-C vs. Substrate Bias

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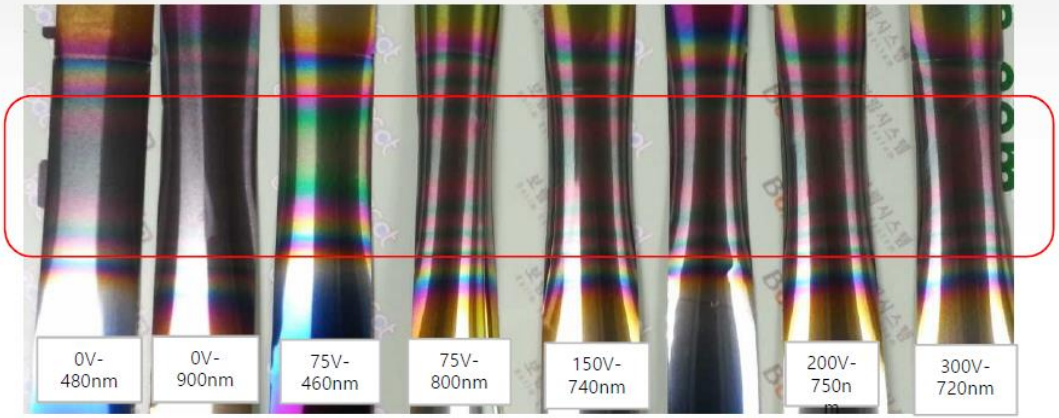
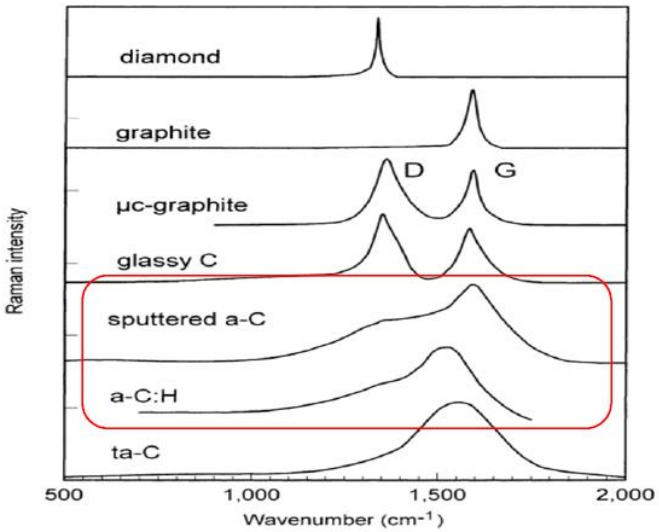
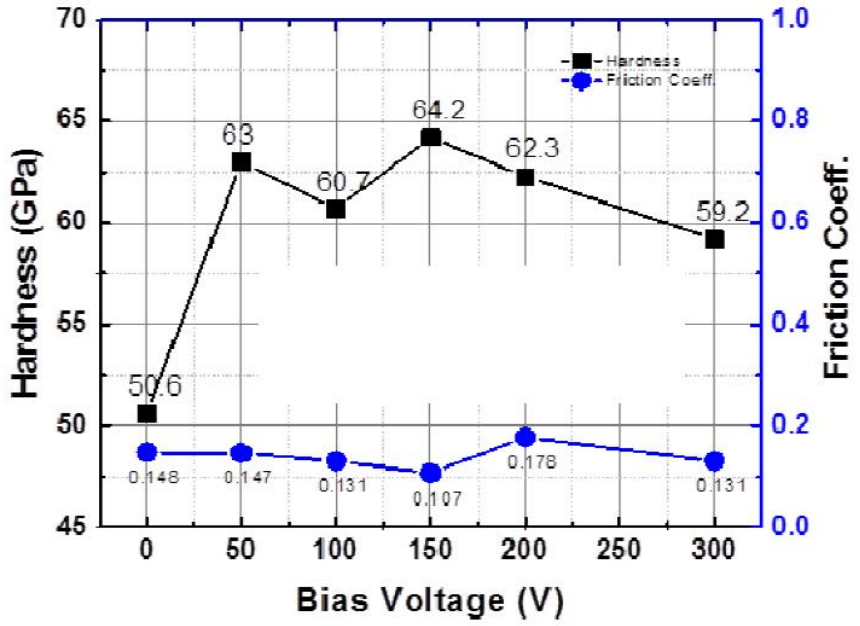
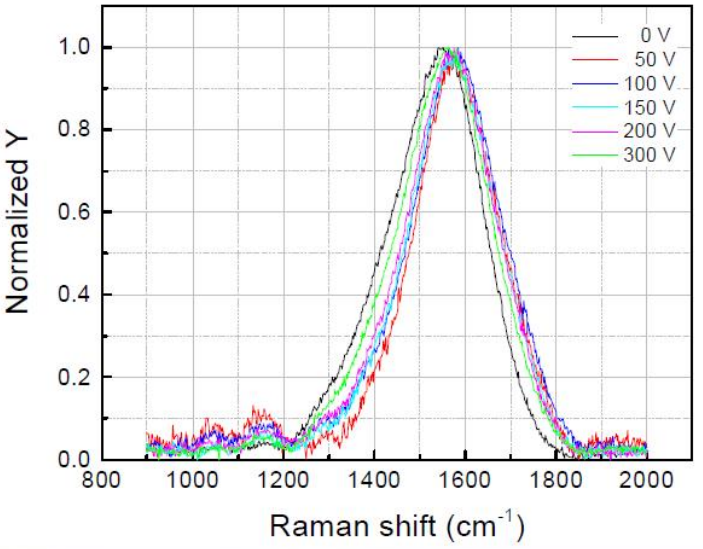
Substrate : Al sheet Asymmetric Bipolar Bias







800nm



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Substrate Bias Effect

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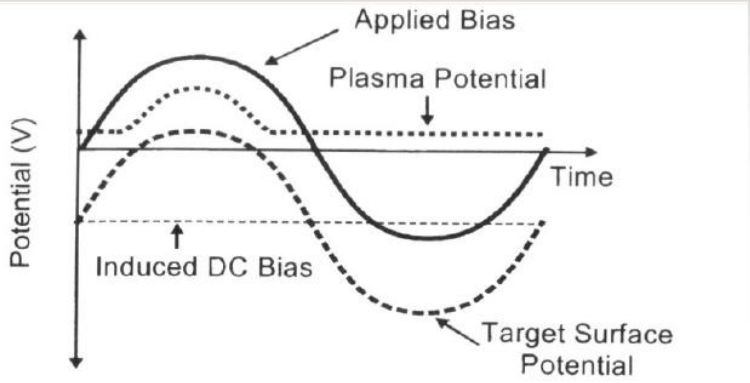
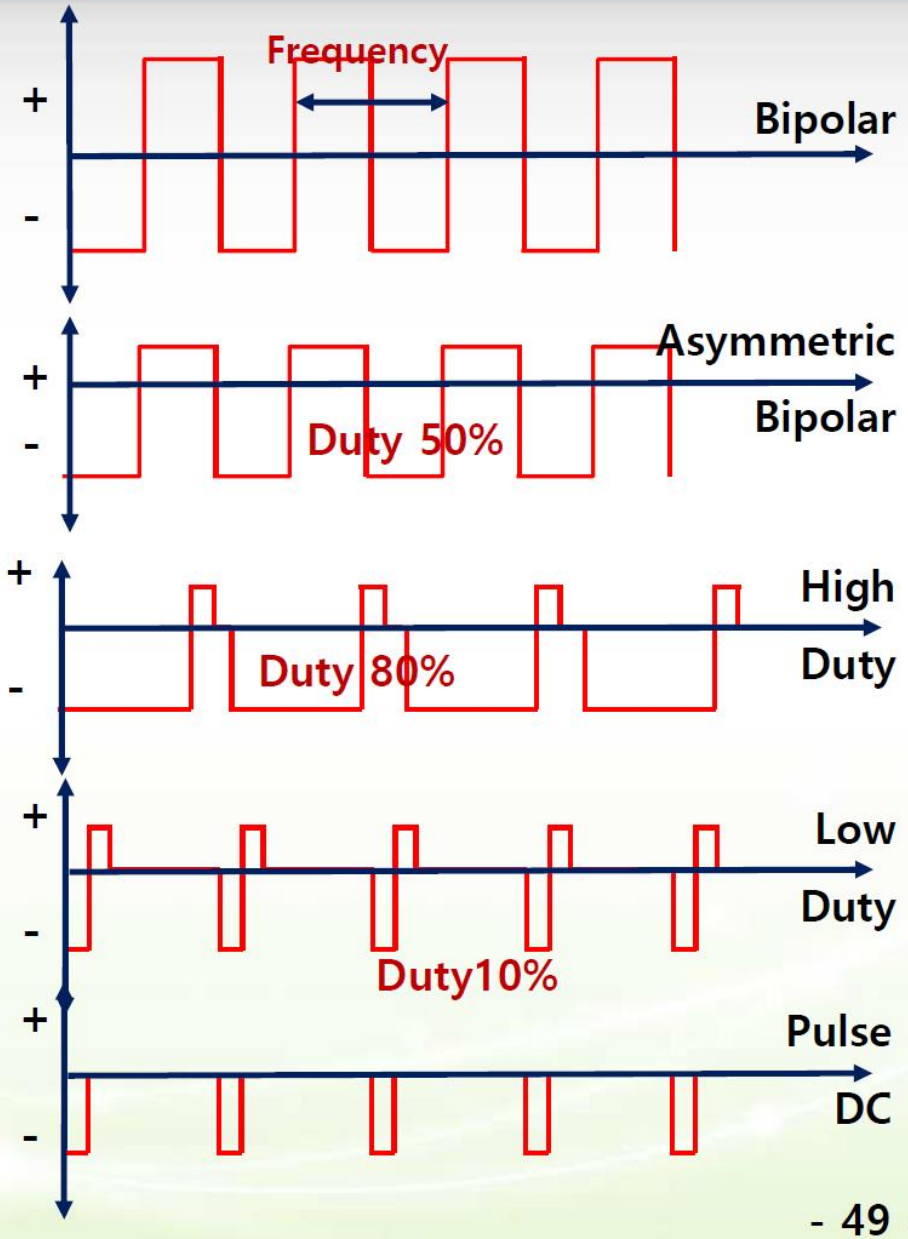


Figure 8: Qualitative temporal evolution of the applied ac bias, the potential at the surface of the target, the plasma potential, and the induced dc bias on the surface of the target.

- DC Substrate Charging ➔ arcing ➔ film damage
- Pulse : DLC and ta-C ➔ insulator
- Or Asymmetric bipolar
- AE : pinnacle PS : 5 ~ 350kHz (duty2.5 ~ 60%)
- EN-tech : MF 5kHz ~ 50kHz , duty max 90%
- PSP : 5kHz ~ 100kHz (duty 5 ~ 65%)
- NTI HV PS : 1500V Max 5% Duty



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Reaction of Substrate by Ion Particle

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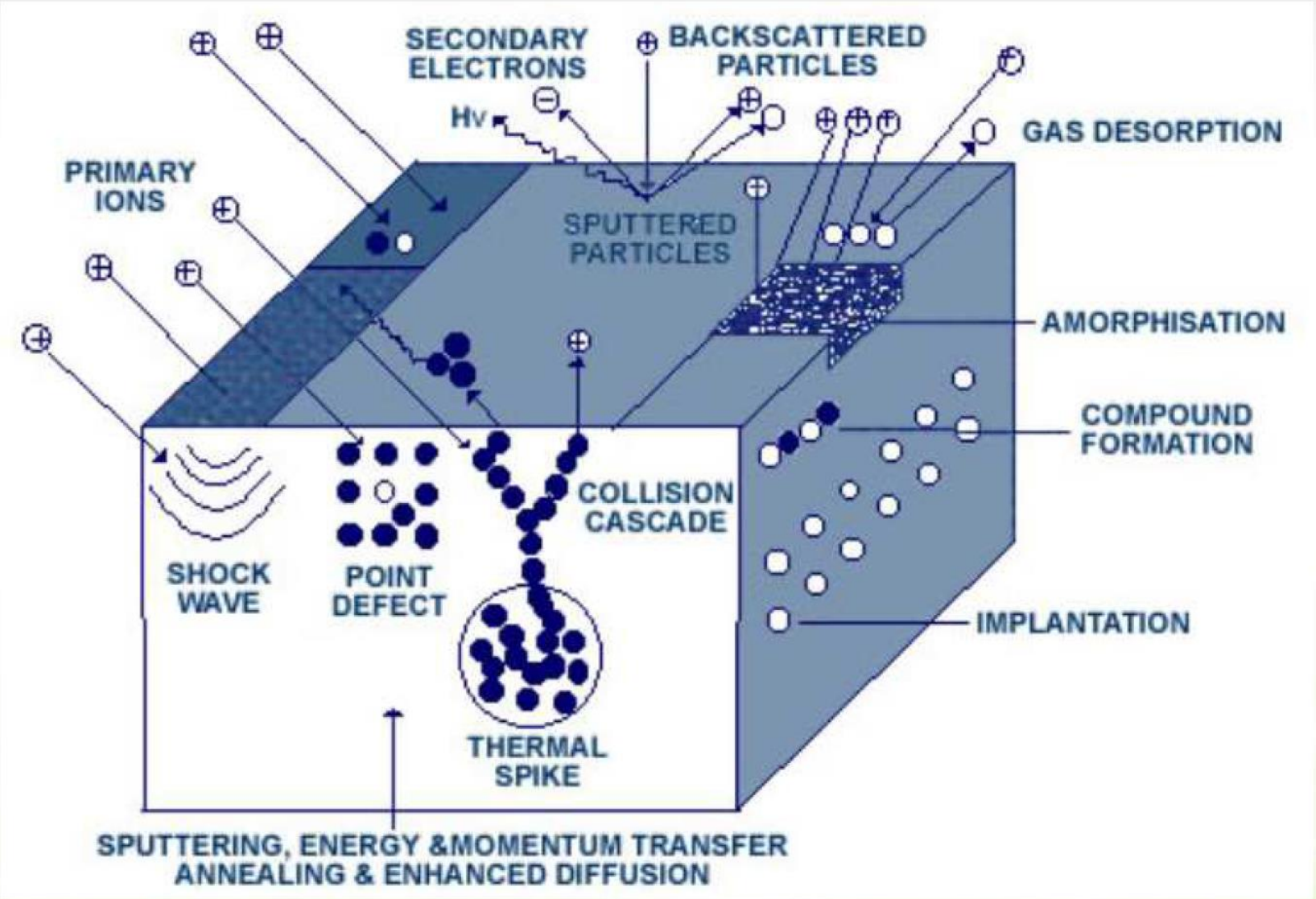

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Crystallization VS. Frequency

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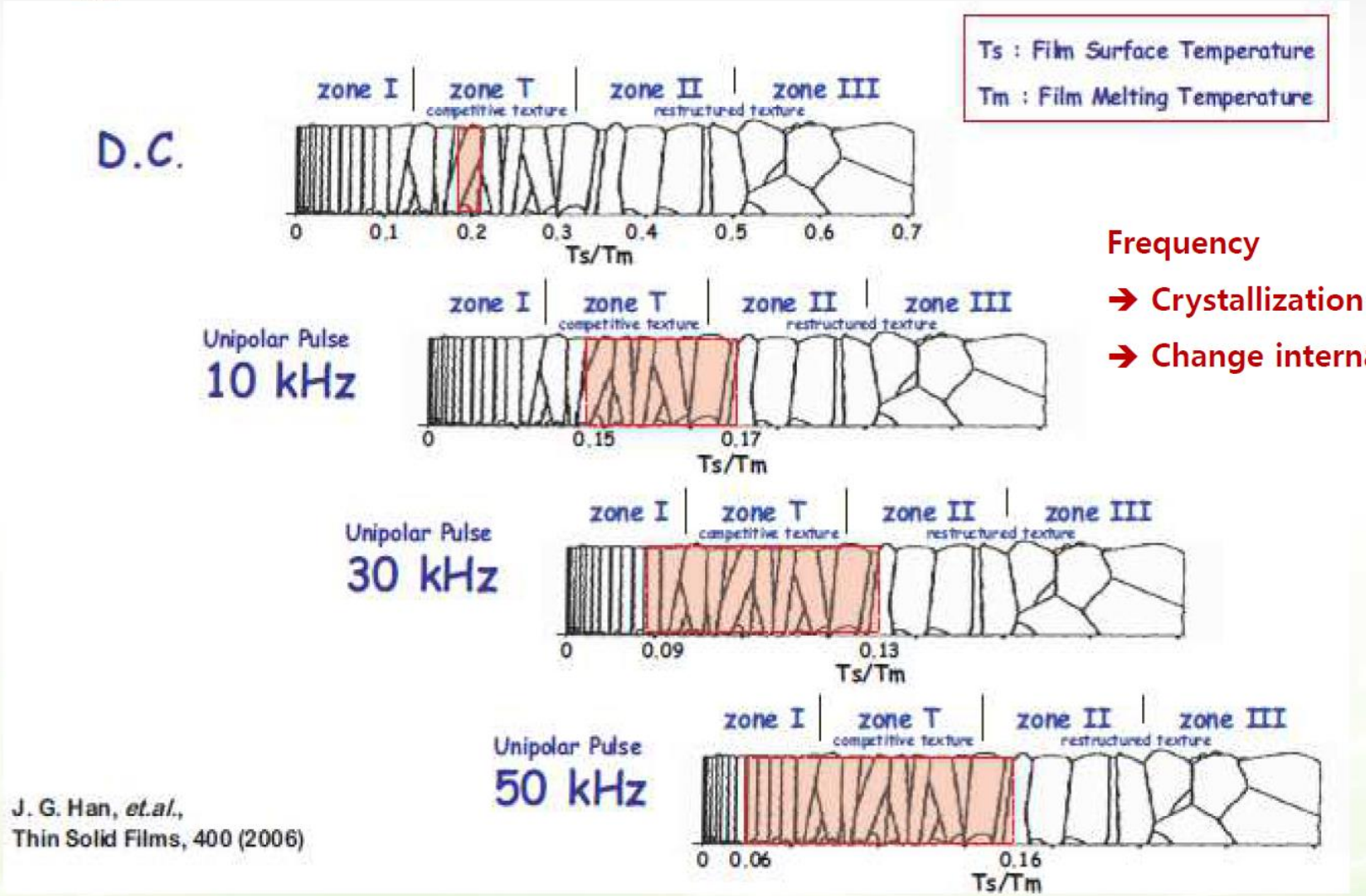
전원 주파수 변화에 따른 막의 결정화 영역 변화



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Substrate selectivity of Film Deposition

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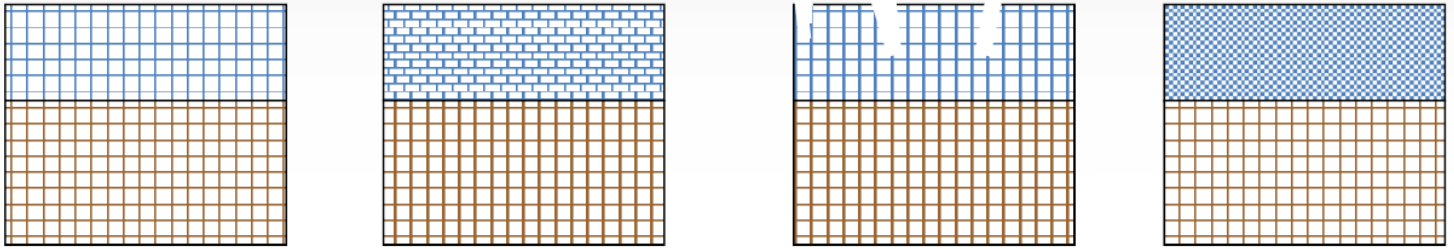
열 팽창에 따른 엇갈림
(Thermal Expansion Mismatch)



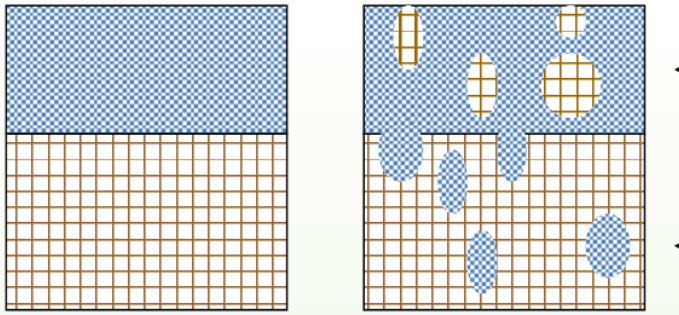
Ideal Case

Thin Film > Substrate
Tensile Stress

Film is thick or brittle
Cracking

Thin Film < Substrate
Compressive Stress

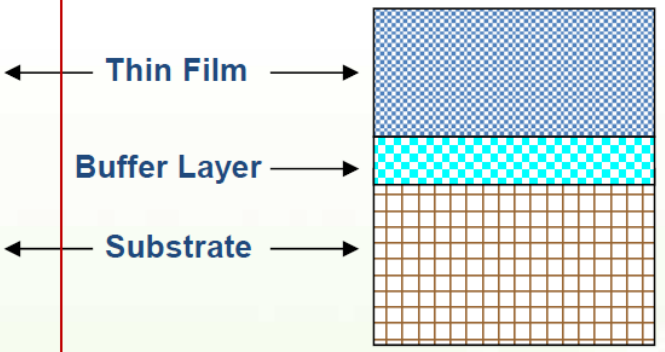
화학적 적합성
(Chemical Compatibility)



No
Chemical Interaction
Inter-diffusion

Undesirable Properties

중간 격리층
(Buffer Layers)



Alleviate a variety of problems such as
Chemical incompativility, Thermal or lattice mismatch

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Substrate selectivity of Film Deposition

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EFFECT \ ISSUE	Chemical Compatibility	Thermal Expansion Match	Surface Quality	Substrate Cleanliness	Substrate Homogeneity	Substrate Thermal Stability	Buffer Layer
Maximum Processing Temperature							
Reacted Layer at interface							
Impurity in Film							
Impurity in Substrate							
Film Adhesion							
Film Bucking/Cracking							
Film Microstructure							
Film Composition							
Film Morphology							
Film Uniformity							
Electro-Magnetic Properties							

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Optimum Film Coatings

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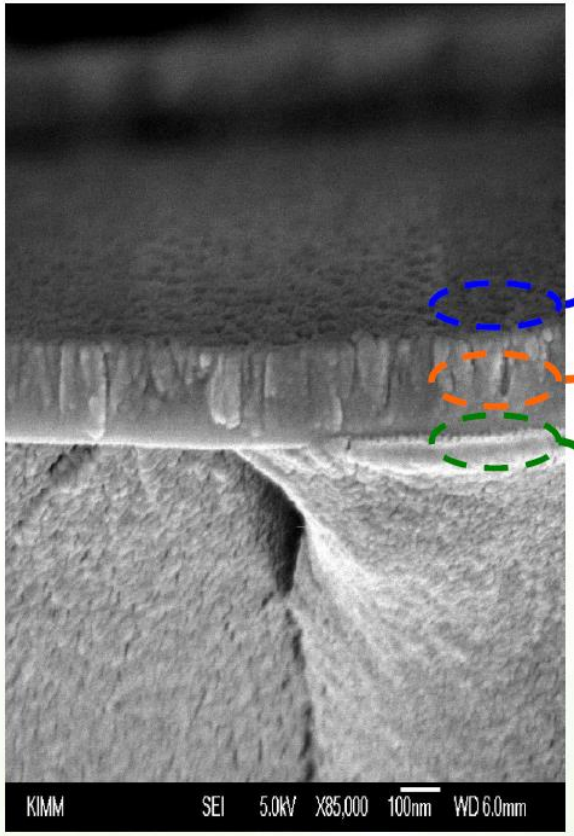
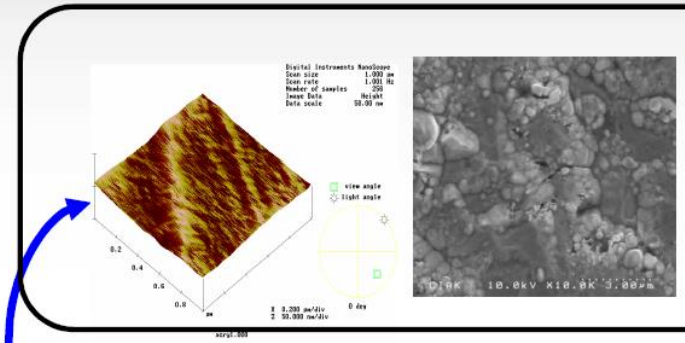
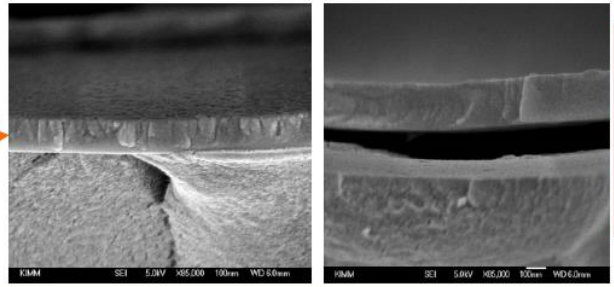
Coating Film





Surface Control
- Surface Roughness
- Surface Properties



Phase Control
- Crystallinity Control
- Nanostructure Films

Interface Control
- Diffusion Layer
- Gradient Interface
- Buffer Layer

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